IN THE CLAIMS

Please enter the below claim amendments.

1. (Currently Amended) An apparatus, comprising:

a memory device including a block of memory operable to store data, said memory device being adapted to at least partially erase said block of memory in a first erase cycle and in a second erase cycle subsequent to the first erase cycle, ~~said memory device being further adapted to determine an erase performance for said block of memory during the first erase cycle,~~ said memory device being further adapted to store a first voltage increment threshold count and a second voltage increment threshold count associated with said block of memory, said memory device being further adapted to count a total number of erase pulses applied to said block of memory, said memory device being further adapted to apply an erase pulse to said block of memory during the first and the second erase cycles having an erase pulse voltage level based at least in part on the total number of erase pluses applied to said block of memory, the first voltage increment threshold count, and a second voltage increment threshold count ~~erase performance of said block of memory during the first erase cycle~~.

2. (Currently Amended) The apparatus of claim 1, wherein the erase pulse comprises an initial erase pulse applied to said block of memory during the first~~second~~ erase cycle.

3. (Currently Amended) The apparatus of claim 2, wherein said memory device is further adapted to apply the~~an~~ initial erase pulse to said block of memory during the first erase cycle having an erase pulse voltage level, and wherein the erase pulse voltage level of the initial erase pulse applied to said block of memory during the second erase cycle is greater than the erase pulse voltage level of the initial erase pulse applied to said block of memory during the first erase cycle.

4. (Cancelled)

5. (Previously Presented) The apparatus of claim 1, wherein said memory device is further adapted to apply a plurality of erase pulses to said block of memory during the first erase cycle and to count the number of erase pulses applied to said block of memory during the first erase cycle, said memory device being further adapted to determine the erase pulse voltage level of the erase pulse applied to said block of memory during the second erase cycle based at least in part on the number of erase pulses applied to said block of memory during the first erase cycle.

6. (Currently Amended) The apparatus of claim 5, wherein said memory device is further adapted to compare the number of erase pulses applied to said block of memory during the first erase cycle to ~~a~~ the first voltage increment threshold count ~~threshold number of erase pulses~~ and to change the erase pulse voltage level of the erase pulse applied to said block of memory during the second erase cycle if the number of erase pulses applied to said block of memory during the first erase cycle is not less than the ~~threshold number of erase pulses~~ first voltage increment threshold count.

7. (Previously Presented) The apparatus of claim 1, wherein said memory device further includes a memory location adapted to store the erase pulse voltage level of the erase pulse, and wherein said memory device is further adapted to store the erase pulse voltage level of the erase pulse in said memory location.

8. (Previously Presented) The apparatus of claim 7, wherein said block of memory comprises a first block of memory and said memory location comprises a first memory location uniquely associated with said first block of memory, wherein said memory device further comprises a second block of memory and a second memory location uniquely associated with said second block of memory, and wherein said second memory location is adapted to store an erase pulse voltage level associated with an erase pulse applied to said second block of memory.

9-16 (Cancelled)

17. (Currently Amended) An apparatus, comprising:

a first block of memory operable to store data and to be at least partially erased in a first erase cycle and in a second erase cycle subsequent to the first erase cycle;

a first memory location uniquely associated with said first block of memory, said first memory location being adapted to store an initial erase pulse voltage level for an erase pulse to be applied to said first block of memory during the second erase cycle, and said first memory location being adapted to store a first voltage increment threshold count and a second voltage increment threshold count associated with said first block of memory;

a second block of memory operable to store data and to be at least partially erased in a first erase cycle and in a second erase cycle subsequent to the first erase cycle;

a second memory location uniquely associated with said second block of memory, said second memory location being adapted to store an initial erase pulse voltage level for an erase pulse to be applied to said second block of memory during the second erase cycle, and said second memory location being adapted to store a first voltage increment threshold count and a second voltage increment threshold count associated with said second block of memory; and,

a processing unit adapted to evaluate erase performance of said first block of memory during the first erase cycle therefor and to evaluate erase performance of said second block of memory during the first erase cycle therefor, said processing unit being further adapted to establish and store the initial erase pulse voltage level of the erase pulse applied to said first block of memory based at least in part on the evaluated erase performance of said first block of memory, and said processing unit being further adapted to establish and store the initial erase pulse voltage level of the erase pulse applied to said second block of memory based at least in part on the evaluated erase performance of said second block of memory.

18. (Previously Presented) The apparatus of claim 17, wherein the initial erase pulse voltage level for an erase pulse to be applied to said first block of memory during the second erase cycle thereof is different than the initial erase pulse voltage level for an erase pulse to be applied to said second block of memory during the second erase cycle thereof.

19. (Previously Presented) The apparatus of claim 17, wherein said apparatus further comprises a voltage source operable to apply erase pulses having respective desired erase pulse voltage levels to said first block of memory and to said second block of memory in response to signals received from said processing unit.

20. (Currently Amended) The apparatus of claim 17, wherein said processing unit is further adapted to count erase pulses applied to said first block of memory during the first erase cycle thereof in order to evaluate erase performance of said first block of memory and to compare the count to the associated first voltage increments threshold value in order to determine whether to increase the initial erase pulse voltage for an erase pulse to be applied to said first block of memory during the second erase cycle thereof, and wherein said processing unit is further adapted to count erase pulses applied to said second block of memory during the first erase cycle thereof in order to evaluate erase performance of said second block of memory and to compare the count to athe associated first voltage increment threshold value in order to determine whether to increase the initial erase pulse voltage for an erase pulse to be applied to said second block of memory during the second erase cycle thereof.

21. (New) A method for determining the erase performance of a block of memory of a memory device, comprising:

counting a number of erase pulses applied to the block of memory during a first erase cycle;

comparing the number of erase pulses applied to the block of memory during the first erase cycle to a first threshold number of erase pulses;

changing an erase pulse voltage level of the erase pulse applied to the block of memory during a second erase cycle if the number of erase pulses applied to the block of memory during the first erase cycle is not less than the first threshold number of erase pulses;

comparing the number of erase pulses applied to the block of memory during the second erase cycle to a second threshold number of erase pulses; and,

changing the erase pulse voltage level of the erase pulse applied to the block of memory during a third erase cycle if the number of erase pulses applied to the block of memory during the second erase cycle is not less than the second threshold number of erase pulses.

22. (New) The method of claim 21, wherein determining the erase performance of the block of memory comprises monitoring the amount of time required to erase the block of memory during the first erase cycle.

23. (New) The method of claim 21, wherein the erase pulse voltage level comprises an initial erase pulse voltage level.

24. (New) The method of claim 21, wherein the method further comprises, if the erase pulse voltage level is set, storing the erase pulse voltage level of the erase pulse in a memory location uniquely associated with the block of memory.

25. (New) The apparatus of claim 6, wherein said memory device is further adapted to compare the number of erase pulses applied to said block of memory during the second erase cycle to the second voltage increment threshold count and to change the erase pulse voltage level of the erase pulse applied to said block of memory during subsequent erase cycles if the number of erase pulses applied to said block of memory during the second erase cycle is not less than the second voltage increment threshold count.